ELECTRONIC INDUSTRY CITIZENSHIP COALITION

Standardizing Methods for Performing Allocation of Supplier Carbon Data for IT Products

Product Carbon Footprinting Allocation Project Results

June 2014

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Abstract

Understanding the total carbon footprint of IT products is important to our customers, policy makers, and stakeholders. However, obtaining accurate, up-to-date carbon data that is used in a product carbon footprinting calculation is often difficult for two reasons: 1 – there is no standardized method for collecting and allocating facility-level data for suppliers; 2 – generic life cycle assessment (LCA) databases contain significant data gaps and are often outdated or unrepresentative. In order to improve data collection in the IT space, a group of companies, along with academia, initiated a project to develop standardized processes for collecting primary product environmental data that builds upon the current EICC (Electronic Industry Citizenship Coalition) Carbon and Water Reporting System. The goal of this project is to develop product-specific allocation methods that link facility-wide environmental data to the specific product types being made within that facility. This paper provides readers with state-of-the-art allocation methods for several IT product subassemblies: ICs, LCDs, PCAs, HDDs, PCBs.

Keywords: product carbon footprinting, data collection method, ICs, LCDs, PCAs, HDDs, PCBs

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Project Background

The total carbon footprint of IT products is becoming more important to our customers, policy makers, and stakeholders. Several countries have initiated voluntary product carbon footprint (PCF) labels; others are currently considering making PCF calculations a requirement for government procurement. In addition, we are beginning to see customer requests for PCF information in bids and tenders. The ICT sector strives to be proactive in our product carbon footprinting efforts and supports reducing the environmental impact of our products.

Challenges

However, two issues with present-day environmental impact data hinder our industry's ability to provide accurate product environmental footprints:

- Data from suppliers is often burdensome to collect for all involved and difficult to use, due to the lack of standardized methods for:
    - collection
    - performing allocation; and
    - reporting this information.
- When supplier data is unavailable, generic life cycle assessment (LCA) databases must be used. However, these LCA databases have shortcomings such as:
    - they contain significant data gaps;
    - available data contains a great deal of uncertainty; and
    - existing data is often outdated.

Improvement Opportunity

To improve our ability to accurately assess the impacts of our products, the IT industry must be able to obtain up-to-date, accurate, and consistent environmental data from our suppliers for our major components. To accomplish this, a group of companies, along with academia, initiated a project to develop standardized processes for collecting primary product environmental data that builds upon the current EICC (Electronic Industry Citizenship Coalition) Carbon and Water Reporting System. The goal of this project is to develop product-specific allocation methods that link facility-wide environmental data to the specific product types being made within that facility (see Figure 1).

Future goals may include developing training modules for suppliers to assist them in collecting data, as well as making a determination as to whether the EICC's Carbon and Water Reporting system would be amenable to incorporating this information.

Benefits

The benefits of a standardized allocation method that uses facility-level data are as follows:

- allows companies to collect up-to-date, consistent data on the environmental impacts of specific products/components
- reduces the reporting burden on suppliers, as most already collect facility-level environmental data and therefore will not have to provide product-specific information
- accurate, consistent data will improve a company's ability to assess uncertainty as well as improve its ability to compare products
- it will improve companies' abilities to truly evaluate product 'hotspots' which can lead to other collaborative efforts to reduce impacts within the supply chains.

Included Products

The initial products included in this assessment were:

- integrated circuits (ICs)
- bare printed circuit boards (PCBs)

- assembly and test of printed circuit boards
- hard disk drives (HDDs); and
- liquid-crystal display (LCD) panels

Allocation Definition

According to the GHG Protocol, “Allocation is the process of partitioning GHG emissions from a single facility or other system (e.g., activity, vehicle, production line, business unit, etc.) among its various outputs.” The GHG Protocol calls for companies to avoid allocation whenever possible as it adds uncertainty to the emissions estimates and especially becomes inaccurate depending on the number and variety of products at the factory. In addition, some of the most popular allocation methodologies are done based on a product’s weight or cost, which may not accurately reflect how overall facility data should be allocated to a specific product type.

In order to obtain improved product environmental footprint data, the IT industry must evaluate how allocation can best be accomplished for each major product/component category instead of using the same approach for all. This project focused on understanding the manufacturing process of the major IT products/components in order to develop product/component-specific allocation algorithms (see Figure 1 below).

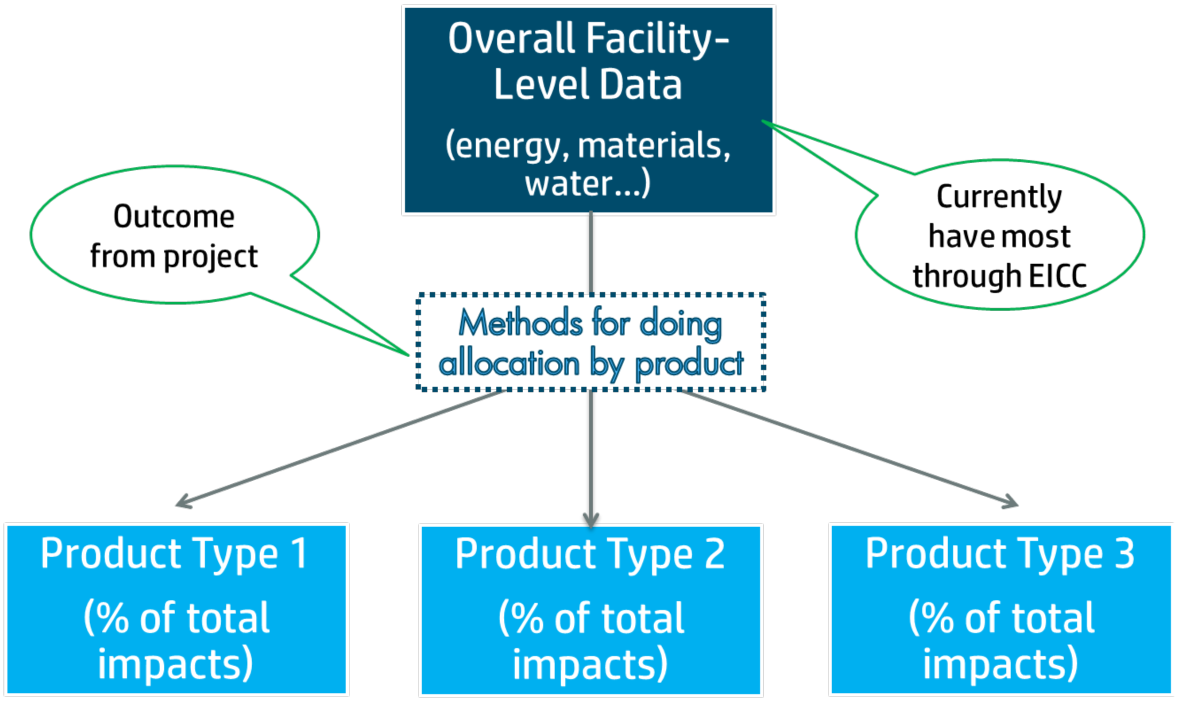


Figure 1- Allocation diagram

Allocation Methodology: Hard Disk Drives

Background

When produced in any volume, hard disk drives (HDDs) are always manufactured in dedicated facilities due to their stringent quality and cleanliness requirements. In this process, precision cleaning and assembly of parts are performed in cleanroom environments, while test, customer-configuration operations, labeling, and pack-out are performed in facilities controlled for temperature, humidity, and electrostatic discharge control but not in cleanrooms. The vast majority of hard disk drives produced today come in either 3.5” or 2.5” disk size form factors, with the number of disks in each device generally varying between one and four. Solid state drives are not included in this analysis because their manufacturing process more closely resembles PCBAs, addressed later in this paper, than the traditional HDD process analyzed for allocation methodology here.

Hard Disk Drive Life Cycle Characteristics

Typical system boundary schemes for a hard disk drive

The system boundaries for hard disk drive factory allocation includes all assembly- and test-related resource inputs, from placing parts inventory onto the production line to final pack-out of finished products, including labeling the outbound packaging. Factory lighting and air conditioning would be included; as of course would operation of high efficiency particle attenuation systems in cleanrooms. Warehousing of parts in nearby Just-In-Time hubs would not be included.

Known emissions hotspots in the hard disk drive life cycle

Hard disk drive assembly and test operations involve the following resource consumption activities:

- Final test media scanning and flaw-mapping (media certification) can take weeks depending on the capacity of the drive; this process consumes the majority of the electricity expended in the end-to-end disk drive manufacturing operation. This is a highly automated process in temperature-controlled conditions where every bit location on every disk is written to and read back to ensure operation.
- Assembly of the HDD is completely automated and usually takes less than a minute per drive. It involves the assembly multiple disks into a hermetically sealed complete HDD product.
- Although most parts enter the hard disk drive manufacturing facility in ready to assemble condition, some precision cleaning of mechanical parts occurs, usually involving aqueous cleaning systems. These systems consume electricity, water, certain cleaning chemicals, and water cleaning/purification/recycling systems, all of which fall within scope of resource allocation calculations, although their impact is proportional to their extent of use.

Hard Disk Drive Manufacturing Facilities

Defining characteristics of facilities that manufacture hard disk drives

As noted above, hard disk drive manufacturing facilities consist of high-volume, high-automation plants dedicated 100% to their intended purpose.

Ways in which allocation is typically performed

There are several methods for allocating facility information to hard disk drives. Allocation may use any of the following as the basis for the denominator when performing the allocations:

- mass of products produced (per mass unit)
- hard disk drive device (per drive)
- units of memory produced (per gigabyte or terabyte)
- number of disks within the drive (per disk)

Challenges associated with the above approaches to allocation

- Per Mass Unit: this is not the best method for performing allocation for HDDs as test rack is the largest energy sink and it is not directly relatable to weight. As test time increases, weight does not necessarily increase.
- Per Drive: same as above – a drive is not directly relatable to test rack time.
- Per Unit of Memory produced – this is directly relatable to test rack time and is a good way to perform allocation. However, the total amount of memory produced is not inherently tracked at the factory level.
- Per Disk – this is also directly relatable to test rack time as the amount of memory on a disk is fixed (i.e. at the time this document was written, 2.5" disks had 500GB, and 3.5" disks had 1TB) and memory is directly correlated to test rack time. In addition, the number of disks built into drives is tracked at the factory level.

Conclusion: Preferred Facility-Level Allocation Method for HDD Manufacturing

As mentioned above, test rack time is by far the most energy intensive process in the manufacturing of an HDD, and test rack time is directly related to HDD memory. Weight is not a factor in manufacturing because the equipment operates the same, independent of product size. Therefore, HDD memory can be used as the single attribute for performing allocation of facility energy use.

The only issue with using memory is that most facilities do not measure the total amount of memory being produced within a given factory. However, facilities do track the total number of disks that are built into drives, which is correlated, to amount of memory produced. Therefore, to perform allocation of overall facility energy/GHG data to a specific HDD made in the facility one should use: the ***number of disks*** of each form factor being built into drives at that facility.

Consequently, the total manufacturing carbon footprint equation for an HDD is as follows:

$$\mathbf{MCF_{HDD}\ (kg\ CO2e)} = GHG_F\ \mathbf{/}\ [(D_{2.5''} * C_{2.5''}) + (D_{3.5''} * C_{3.5''})] * M_{HDD}$$

where…

MCF_{HDD} = the manufacturing carbon footprint of a single HDD (kg CO2e)

GHG_F = the total manufacturing facility greenhouse gas emissions in a year (kg CO2e)

$D_{2.5''}$ = the total number of 2.5" disks produced within the factory in a year

$C_{2.5''}$ = the current total capacity of a 2.5" HDD (in Terabytes)

$D_{3.5''}$ = the total number of 3.5" disks produced within the factory in a year

$C_{3.5''}$ = the current total capacity of a 3.5" HDD (in Terabytes)

M_{HDD} = the total memory of a specific HDD (in Terabytes)

Other Considerations for HDDs

The total cradle-to-gate carbon footprint of an HDD is made up two main components:

- upstream processes (extraction, component manufacturing, transportation, etc.); and
- manufacturing and test.

The upstream processes can be as high as 80% of the total HDD footprint so just performing the allocation on the factory emissions could leave out a significant portion of the footprint. For upstream manufacturing, the processes with the largest carbon impact are the electronics, disks and motor.

The purpose of this document is to standardize the manufacturing portion of a product's carbon footprint. However, the upstream portion of the carbon footprint is also very important and should also be considered if the full impact of a product is to be measured.

Since the electronics, disks, and motor are the biggest impacts, these should be considered when calculating the upstream portion of the cradle-to-gate PCF for an HDD.

Therefore, the total cradle-to gate carbon footprint equation for an HDD is as follows:

Total Cradle-to-Gate PCF of HDD (kg CO2e) = $MCF_{HDD} + UCF_{HDD}$

where…

UCF_{HDD} (kg CO2e) = $(CF_e * W_e) + (CF_d * W_d) + (CF_m * W_m)$

and where…

UCF_{HDD} = the upstream carbon footprint of a single HDD (kg CO2e)

CF_e = average carbon footprint of electronics per kg of electronics from LCI database (kg CO2e/kg electronics)

W_e = total weight of the electronics within the HDD

CF_d = average carbon footprint of disk per kg of disk from LCI database (kg CO2e/kg disk)

W_d = total weight of the disks within the HDD

CF_m = average carbon footprint of motor per kg of motor from LCI database (kg CO2e/kg motor)

W_m = total weight of the motor within the HDD

Allocation Methodology: Liquid Crystal Displays (LCDs)

Background

This section provides an overview of issues related to the allocation of facility-level environmental data to an individual product class for products including Liquid Crystal Display technology. Such products could include anything with a display such as monitors, televisions, notebooks, tablets and phones. The unit of interest in this allocation discussion is the LCD module by itself rather than the final end product. Environmental footprinting for LCDs requires inputs from several types of facilities; the focus of this document is energy used and emissions generated in the array and cell manufacturing facility as well as the module assembly facility. There are also many upstream raw materials and electronic components included in the device that are referenced under “other considerations” below.

LCD Life Cycle Characteristics

Typical system boundary schemes for an LCD module

The calculated life cycle system boundary typically starts with the input of the borosilicate glass and related raw materials and ends with the completed LCD module containing the frame, and primary electronics. Depending on the application of the module it is then integrated into a larger device such as a notebook, all-in-one, or mobile. Otherwise, housing is added to complete the product in the case of a television or monitor.

Known emissions hotspots in the LCD life cycle

To date, the observed emissions hotspots for the LCD module include the electricity in array and cell fabrication. Another potential hotspot is fugitive emissions from PFC gases depending on how much abatement occurs at a facility. Electronics are also an important hotspot if the full display product is considered.

LCD Manufacturing Facilities

Defining characteristics of facilities that manufacture LCD modules

Typically manufacturers that make LCD displays will manufacture the array and cell in one facility and perform module assembly in another. This is not always the case. Sometimes assemble takes place within the same facility. Sometimes module assembly is performed by a different company.

The array and cell facilities take in large pieces of glass, and these pieces of glass are typically cut in the beginning of the module process. The size of the incoming piece of glass is dependent on the generation of the plant. A single facility produces several different sized and types of products; often the newer facilities manufacture larger products such as televisions and the older ones make monitors and notebooks. Generation refers to each glass size that can be handled within a particular facility. For example, generation 10 array and cell facilities can manufacture 2,880 x 3,130 mm sheets of processed input glass. As a result more products can be made per input sheet.

Ways in which allocation is typically performed

For array and cell facilities, allocation (or normalization of the facility environmental data) is typically performed by the area of input sheet ($kgCO_2/m^2$ input sheet, for example) put into the production facility, where the facility is specified by generation. Most typically there are two processes related to the input glass, one for the color filter and one for the thin film transistor (TFT) array glass.

For module facilities, area is likely still the correct measure for allocation. Even though the LCD modules are essentially acting as units now, the larger units may require more time in testing. The most critical factor to identify for this proposed allocation is whether the incoming glass is cut to a finished size or uncut and remaining in sheet form.

Challenges associated with the above approaches to allocation

For the calculation to be done correctly, one needs to clarify whether the input sheet includes the color filter or not. If the color filter is included that would increase the amount of input sheet that is accounted for. Also scrap should be accounted for in the allocation by proportioning it to the amount of glass that is assumed in the final product. For example, as the products are cut from the input sheet there is waste on the edges when the dimensions of the product do not perfectly add to the total input sheet area.

The following issues were identified with an input glass sheet area-based allocation scheme:

1. The facility level data includes multiple products across a single generation. Because product portfolios are complex and vary significantly over the year, allocation to product types just by generation of facility may not be accurate. In order to determine if this is a problem, look at the nature of the variation. If the portfolio variation occurs uniformly, in other words production levels are changing consistently across products, then the approach might be fine. Otherwise, data may need to be obtained separately for each product type.
2. Boundary definition is another concern because, as mentioned above, some facilities include module assembly while others do not. While important to document, this issue should not skew facility carbon footprint allocation at this point because the module assembly operation is not a significant part of the total burden (either in terms of the percent of the facilities that have more than array and cell and also because the percentage of electricity is small for module assembly in proportion to glass processing, around 5%).
3. A significant issue with the area-based allocation is that for some products multiple passes are required for portions of the manufacturing line. As an example, for in-plane switching technologies and for smart phone products there will be more layers than for other products. In these cases something analogous to mask layers in semiconductor manufacturing would be appropriate. Layer count should be added to the allocation guidance when data are available to support this improvement.

Conclusion: Preferred Facility-Level Allocation Method for LCD Manufacturing

Because most of the processes to make the TFT glass and the color filter scale with area, the area of the input sheet is the most appropriate way to allocate total facility burden to an individual product. However, a modification should be made to account for scrap in this allocation.

Consequently, the total manufacturing carbon footprint equation for an LCD module (LCDM) is as follows:

$$\mathbf{MCF_{LCDM}\ (kg\ CO2e)} = [(GHG_F \,/\, A_{input}) * (A_{LCDM}+A_{scrap})]$$

where…

MCF_{LCDM} = the manufacturing carbon footprint of a single LCD module (kg CO2e)

GHG_F = the total manufacturing facility greenhouse gas emissions in a year (kg CO2e)

A_{input} = the total input glass area (for TFT and color filter) brought into the facility in a year (in m^2)

A_{scrap} = the area of glass scrap (will be a function of the generation and display area)
Note: scrap may not be relevant for module assembly

A_{LCDM} = the total area of a specific LCD (in m^2)

Other Considerations for LCDs

As was mentioned in the hard drive description above, the upstream raw materials may also be significant in the total burden of a product containing an LCD module, particularly when a large number of electronics are included (often the case for televisions). Similar equations can be used for the upstream impact where the components could be broken down into: electronics, backlight unit, cables and housing, and panel materials (glass, films).

Below is a set of questions that can be used to understand whether an area-based allocation metric will be appropriate:

- What is the generation of the array and cell facility? Newer generations might be more indicative of more advanced technology where area based allocation may not be sufficient.
- How many different lines are being run within the facility? Does each line manufacture the same types of products? If not, how are they different? Again, some products may require multiple passes through the line leading to an overestimate for the impact of products that don't.
- Where does cutting of the glass occur? If cutting is within the facility of interest (where the data are being collected) then the scope 2 emissions may be overestimated by an area based allocation.
- What is the variety of sizes of products produced in the module facility? If there is significant variation in the product sizes, scrap will be allocated in a way that overestimates scrap for those products where scrap is a small fraction.
- How many times does the product go through the manufacturing line? This will dictate whether an area-based allocation overestimates the impact.

Allocation Methodology: PCBs

Background

Printed circuit boards are ubiquitous throughout electronic products. The final component that is present in an end-user device is a printed circuit board assembly that includes the board itself as well as both passive and active electronic mounted components such as integrated circuits, capacitors, transistors, resistors, and diodes, among others.

PCB Life Cycle Characteristics

Typical system boundary schemes for a PCB

The boundaries for typical PCB facility begin with preparation of FR4, the glass-reinforced epoxy laminate, and end with the surface finishing of the laminated board. For factories that perform additional services, such as component and hardware installation, an overall factory proportion factor for PCB production versus other operations may need to be derived from available data, because for consistent assessment of the PCB alone, such additional operations are beyond the PCB system boundaries.

The layer count, surface finish and hole technologies will vary by product type. The production of the printed circuit board generally includes the following steps:

1) Core
2) Layering
    a. Dry/Wet film
    b. Develop Etch Strip
    c. Brown oxidation
    d. Pressing/lamination
3) Drilling (Mechanical and/or laser)
4) Desmear
5) Dry film
6) Pattern plating
7) Etching
8) Surface Finishing and Soldermask
9) Routing/punching (contouring)

Known emissions hotspots in the PCB life cycle

For the printed circuit board assembly, the board itself is generally more carbon-intensive, and within the board preparation process, the heating associated with the pressing and lamination steps can consume the most energy. Drilling can also have significant impact where there is particularly complex architecture, although drilling operations typically last only a few minutes per board. A third hotspot is the electroplating process, where panels of circuit boards spend up to an hour in electroplating baths with substantial current consumption taking place both during actual plating and in automated panel lifting and moving steps between the various baths. Although electroplating may consume large amounts of electricity, the process itself allocates well with board size.

Non-energy based fugitive emissions from a facility manufacturing PCBs are typically quite low.

PCB Manufacturing Facilities

Defining characteristics of facilities that manufacture PCBs

PCB facilities typically perform all of the board preparation, surface finishing, and contouring steps. There will be variation in how complete the board is; some facilities may also do some board assembly (component addition) or may omit the final surface finishing or contouring steps, leaving products in panels for ease of subsequent operations.

A facility can be characterized by the average layer count (more sophisticated boards have higher counts). There is a very dramatic range in the facilities that make boards, but increasing layer count generally accompanies greater complexity of other features, such that layer count emerges as the single predominant allocation variable after board size and can be used to incorporate the other accompanying complexity factors. Still, other characteristics such as the percentage of sequential lamination, back drilling, and high density interconnect (HDI) technology impact the PCB carbon footprint to the extent that they must be acknowledged.

Ways in which allocation is typically performed

Allocation is performed most typically by **board area** and **layer area** (final board area * number of layers).

Challenges associated with the above approaches to allocation

There are several steps in the process of PCB manufacture that happen to each layer (imaging, etching, etch resist stripping, etc.) and several steps that happen to the board as a whole (lamination, pattern plating, surface finishing). Therefore, performing allocation just by board area or just by layer area is not recommended.

If sequential lamination (a process that essentially breaks the board into 3 standard boards depending on the final board layer count) is performed, an additional correction factor for energy consumption may need to be applied to differentiate sequential lamination from single lamination processes.

Conclusion: Preferred Facility-Level Allocation Method for PCB Manufacturing

The ideal approach to allocation would include dividing the production process into those steps that occur on layers and those that occur after the last layer lamination process. Another valuable way to allocate would be segmenting into steps applied to outer layers and steps applied to inner layers. Neither of these approaches is feasible for most facilities, as metering is not performed on this fine scale. Therefore two modified allocation strategies are presented.

The simplest way to allocate carbon footprint impact for PCB, and the recommended way in the absence of more detailed energy consumption data, is by total area of layers. The total manufacturing carbon footprint for the PCB is therefore:

$$\mathbf{MCF_{PCB}\ (kg\ CO2e)} = [GHG_F \,\mathbf{/}\, (A_{layer\_total})] * (A_{PCB\_Board} * L_{PCB})$$

where…

MCF_{PCB} = the manufacturing carbon footprint of a single PCB in a product (kg CO2e)

GHG_F = the total manufacturing facility greenhouse gas emissions in a year (kg CO2e)

A_{layer_total} = the total area of layers of board produced in the facility for that year (in m^2)

A_{PCB_Board} = the specific PCB board area for the product being studied (in m^2)

L_{PCB} = the layers of PCB for the product being studied

An improved allocation technique that may be possible for some facilities is to allocate the electricity by layer area and the fuel used in heating by board area. Most heating processes use gas or other fuel that is tracked separately from electricity. And the lamination step is a heating step. This implies that Scope 1 emissions would be allocated by board area and Scope 2 emissions by layer area.

Consequently, the total manufacturing carbon footprint equation for a PCB is as follows:

$$\mathbf{MCF_{PCB}\ (kg\ CO2e)} = [GHG_{scope1} \,\mathbf{/}\, (A_{board\_total})] * (A_{PCB\_Board}) + [GHG_{scope2} \,\mathbf{/}\, (A_{layer\_total})] * (A_{PCB\_Board} * L_{PCB})$$

where…

MCF_{PCB} = the manufacturing carbon footprint of a single PCB in a product (kg CO2e)

GHG_{scope1} = the total Scope 1 manufacturing facility greenhouse gas emissions in a year (kg CO2e)

GHG_{scope2} = the total Scope 2 manufacturing facility greenhouse gas emissions in a year (kg CO2e)

A_{layer_total} = the total area of layers (inner and outer) of board produced in the facility in that year (in m^2)

A_{board_total} = the total area of board produced in the facility in that year (in m^2)

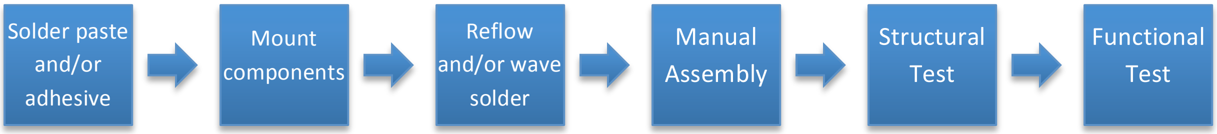
A_{PCB_Board} = the specific PCB board area for the product being studied (in m^2)

L_{PCB} = the layers of PCB for the product being studied

Allocation Methodology: PCA Assembly and Test

Background

Contract manufacturing facilities often perform the activity of taking a bare circuit board and the components of an ICT (Information and Communication Technology) product, mounting the components to the board, permanently securing the components with solder and/or adhesive, possibly singulating panels of products into finished items, and testing the products in one or more ways. Assembly and test describe the two major manufacturing steps that transform many parts into one conjoined assembly ready for use. The final product of the assembly process is known as a "printed circuit assembly" (PCA), or a "printed circuit board assembly" (PCBA). The basic steps for electronics assembly and test are as follows. Note that repair activities are not included in this flow:



PCA Assembly and Test Life Cycle Characteristics

Typical system boundary schemes for Printed Circuit Assembly and Test

The typical system boundaries for PCA Assembly and test begin at the electronics-manufacturing site, where all of the required component materials for assembly have been staged; these components are typically a bare circuit board, electronic components such as capacitors, resistors and semiconductors (or Integrated Circuits), and many other materials. The carbon footprint impact of these components and materials is not considered in this calculation. Rather, the calculation is the "transformation" of parts and materials into finished goods. The boundary for printed circuit board assembly and test ends at a 'functional test' or a 'final system test', where the product is completed, tested, and ready for pack-out and shipping.

Known emissions hotspots in the PCA life cycle

While emissions hotspots will vary based on the different types of assembly and test processes involved, the observed emissions hotspots for PCBA assembly and test include the electricity consumption in the "reflow" and/or wave solder processes (where the board with all of its placed components are heated to a temperature where the solder will melt). Another potential hotspot is at the 'run-in' or 'burn-in' testing, where the product itself is operated either at ambient temperature or in an electrically heated chamber for hours.

Printed Circuit Assembly and Test Facilities

Defining characteristics of facilities that perform printed circuit assembly and test

Assembly Processes

The assembly process can vary. A product may have all surface-mount components, which would require only surface mount assembly, or a product may have through-hole components, which would require a wave solder process. In general for most modern ICT products, there would be a combination of surface mount and wave solder processes, with up to 90% of the product using surface mount technology. However, items such as power supplies may utilize more through-hole components, which would rely on more hand assembly and wave solder processes. Many complex assemblies feature components on both sides of the board, which usually requires adhesives on at least one side of the board, and then often a combination of both reflow and wave soldering.

Test Processes

As with assembly, the test process varies based primarily on the product's cost and complexity. In addition, test processes can vary *greatly* based on the technology genre that the product performs. For example, the product that utilizes optical technologies may require optical tests, which often require substantial set-up time to perform. Higher complexity products typically tend to go through both an in-circuit test and a functional 'run-in' or 'burn-in' test in which the product is put into a thermal chamber and run in normal operation in an higher-than-usual temperature environment for hours. The in-circuit test checks for open and short circuits, discrete component values, basic logic functions, and can also perform firmware loads and initializations. If in-circuit test is included in the test regimen, it precedes functional test. Less complex boards often skip in-circuit testing and sometimes even functional testing. When performing allocation, the energy consumption of all test processes applied to the product must be factored into the calculation.

Ways in which allocation is typically performed

There are several methods for allocating facility carbon footprint to printed circuit assembly and test. Allocation may use any of the following as the basis for the denominator when performing the allocations:

- Mass of products produced (per mass unit)
- Units of products produced (per unit)
- Number of placements, solder joints
- Board complexity index (A calculation based on solder joint and component placement counts)

Challenges associated with the above approaches to allocation

- Per Mass Unit: The approach uses a scale factor associated with the different complexities of products that are manufactured in contract manufacturing facilities; however, there are still challenges to this method:
    - A level of inaccuracy can occur when there is another allocation that is performed. For example, if a facility is shared, a contract manufacturer may commonly allocate emissions to customers by % business first before providing the customer with their share of emissions, which is then allocated by total weight manufactured.
    - PCBA weight information may not be available; however, final product weight can be available. The weight ratio helps in ensuring (as much as possible) that the more accurate weight is considered in the calculation.
- Per Unit: The approach uses a scale factor associated with the different complexities of products that are manufactured in contract manufacturing facilities; however, there are still challenges to this method:
    - A level of inaccuracy can occur when there is another allocation that is performed. For example, if a facility is shared, a contract manufacturer may commonly allocate emissions to customers by % business first before providing the customer with their share of emissions, which is then allocated by total weight manufactured.
    - The manufacturing unit approach ‘averages’ the per unit emissions. Larger products end up with smaller than expected emissions while smaller products end up with larger than expected emissions.
- Number of Component Placements or Solder Joints: this approach uses a basic factor of the number of components placed, or the solder joint count of the PCBA.
    - One inaccuracy is the time it takes to place a small component versus a large component is not the same. More complex devices with many pins take longer for placement than smaller components. For example, a ball grid array device (BGA) can have hundreds and even thousands of pins. Great care has to be taken by the surface mount machine to ensure correct placement. However, small components such as a resistor or a capacitor typically have two pins and are easier to place. Products will vary greatly in terms of the mix of small and large components; therefore, a basic impact per component allocation may generate inaccuracies for both large and small products. For this reason an allocation based on the number of solder joints is preferred if the data is available.
    - Another challenge is the availability of data. It becomes a daunting task to understand the number of components that are placed on each different type of product that the facility manufacturers, and then the volume of each of the different types of projects in that facility. Furthermore, calculating the number of solder joints on a PCBA adds another level of complexity to the equation: you must know the pin count and quantity of each component on each board type produced. This would require a level of analysis that few suppliers are willing to undertake.

- Board Complexity: this alternative takes into account the number of components and also the solder joints that make up a PCBA. The complexity formula quoted below is the following[1]:

  $$Ci = ((\#C + \#J)/100)) * D * M$$

  Where:

  Ci = Complexity Index

  #C = Number components

  #J = Number of joints

  D = Double sided D = 1 and Single sided D = 0.5

  M = High Mix M = 1 for high mix and M = 0.5 for low mix

  - The challenge to this method is that placement times are still affected by component type and board area. In addition, a board with a high simple component count can have the same complexity index (e.g. all resistors) as a board with a very low but complex component count (e.g. a board with a few large BGAs only). This would show that the impact should be the same if the complexity index calculation was used. Since the impact of placing a BGA is higher, the smaller board with BGA devices would have a larger impact than the larger board with all resistors. Nevertheless, component placement represents only a small fraction of the carbon footprint of the assembly process, while soldering processes represent the lion's share, so this source of inexactness may be negligible.

Conclusion: Preferred Facility-Level Allocation Method for Printed Circuit Assembly and Test

For this study a 'tops-down' approach for facility level allocation was developed and conducted through data collection from contract manufacturing sites in Asia, and physical product-related data such as manufacturing volume, weight, number of placements, etc. was collected from suppliers. Of the possible approaches, the two most scalable approaches that allow for an assembly and test allocation tied to the product turns out to be (a) product weight based, and (b) manufacturing volume based.

For this approach, three major pieces of data are required to allocate facility emissions to the product:

1. Total facility emissions within a certain time period
2. Total weight of PCBAs manufactured in said facility in the same time period
3. Total weight of PCBA that you want to determine an assembly and test carbon footprint for

The following calculation can be used for determining the GHG emissions of a product from facility level information. A key factor is that the actual PCBA weight is required to determine the PCBA assembly and test GHG emissions impact:

$$MCF_{A\&T}\ (kg\ CO2e) = W_{PCBA} * (GHG_F / W_{tot\_PCBA})$$

where…

$MCF_{A\&T}$ = the assembly and test carbon footprint of a specific product (kg CO2e)

GHG_F = the total manufacturing facility greenhouse gas emissions in a year (kg CO2e)

W_{PCBA} = the weight of the specific PCBA that emissions are being determined for (kg)

W_{tot_PCBA} = aggregate **PCBA** weight of all products manufactured in reported year (kg)

Alternatively, if the actual weight of the PCBA is unknown, the formula can be adjusted to the following:

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[1] Oresjo, S. A New Test Strategy For Complex Printed Circuit Board Assemblies, http://www.home.agilent.com/upload/cmc_upload/All/Nepcon99.pdf

$$\mathbf{MCF_{A\&T}\ (kg\ CO2e)} = (W_{FA} * (GHG_F \mathbin{\mathbf{/}} W_{tot})) / PCT_{elec})$$

where…

$MCF_{A\&T}$ = the assembly and test carbon footprint of a specific product (kg CO2e)

GHG_F = the total manufacturing facility greenhouse gas emissions in a year (kg CO2e)

W_{FA} = the **completed** weight of the specific product (kg)

W_{tot} = aggregate **completed** weight of all products manufactured in reported year (kg)

PCT_{elec} = an average percentage of the weight of the electronics only to the total weight of the shipped product

Alternative Method: Manufacturing Volume Approach

An alternative approach is available if one is unable to obtain weight information. For this approach, two major pieces of data are required to allocate facility emissions to the product level:

1. Total facility emissions within a certain time period
2. Total number of units manufactured in said facility in the same time period

With this data, the following formula can be used to calculate the allocated assembly and test emissions tied to the product in question:

$$\mathbf{MCF_{A\&T}\ (kg\ CO2e)} = (GHG_F \mathbin{\mathbf{/}} N_{tot\_PCBA})$$

where…

$MCF_{A\&T}$ = the assembly and test carbon footprint of a specific product (kg CO2e)

GHG_F = total facility greenhouse gas emissions in a year (kg CO2e)

N_{tot_PCBA} = aggregate count of all **PCBA**s manufactured in reported year (kg)

Lastly, a correction factor for energy-intensive test processes such as lengthy high-temperature burn-in should be applied to the allocation calculated with the above formulae. Such a factor would necessarily derive from energy consumption measurement studies of the test processes involved, weighing atypically energy-intensive test processes appropriately higher than the factory's typical ones.

Other Considerations for Printed Circuit Assembly and Test

This allocation method is a 'tops-down' approach to calculating the emissions from assembly and test (gate to gate). This method does not include the materials that are transformed into the final product. Assembly and test may only be a small percentage of the total manufacturing impact (internal studies have shown that assembly and test typically represents between 10% to 20% of the carbon footprint of the finished product cradle-to-gate carbon footprint). To have a complete calculation of the full manufacturing impact, the practitioner should consider the components as well.

In addition, a tops-down approach may aid in calculating the assembly and test portion of an LCA; however, manufacturers should consider using a 'bottoms-up' approach to analyze in detail their assembly and test processes for each product to aid in identification of hotspots and reduction opportunities.

Allocation Methodology: Integrated Circuits (wafer fabrication focus)

Background

Integrated Circuits (ICs) are ubiquitous throughout electronic products. They range quite dramatically in complexity, package type, area and stacking within the die.

IC Life Cycle Characteristics

Typical system boundary schemes for an IC

Typical system boundaries include the emissions from the overall IC manufacturing process, and those emissions are from fuels used in onsite electricity generation systems, as well as purchased electricity consumption. Typically the clean silicon wafer is the input to the fabrication facility, and then the processed wafer or packaged chip, depending on the scope of the facility, is the output. The IC carbon footprint allocation described does not include the packaging of the die into a finished component ready for assembly. This packaging operation (often called back-end) may need to be factored into the calculation of the final integrated circuit product.

Known emissions hotspots in the IC life cycle

The emissions within the manufacturing stage primarily stem from the use of fluorinated compounds in etching and cleaning process steps as well as the electricity purchased to power manufacturing facilities. Process emissions include fluorinated greenhouse gases (F-GHGs) used in plasma etch and chamber cleaning, nitrous oxide (N2O), fluorinated heat transfer fluids (F-HTFs), and refrigerant GHG emissions. The materials also contribute significantly to emissions, namely the highly refined chemicals used in production and high purity silicon substrate. However the latter are not included within the facility Scope 1 and 2 emissions as dictated by the Greenhouse Gas Protocol.

IC Manufacturing Facilities

Defining characteristics of facilities that manufacture ICs

IC manufacturing facilities can include fabrication activities, assembly and test activities, or a combination of the two. Other activities that might take place at a facility include research and development, packaging, water/steam generation, waste/wastewater treatment, office facilities, employee amenities, etc.

Ways in which allocation is typically performed

In some cases, a firm may allocate firm-wide data to a specific product type over a defined time period, regardless of the facility where it was manufactured. More commonly, data is allocated based on area* number of mask layers or number of dies produced over a specific time period in one manufacturing facility.

Challenges associated with the above approaches to allocation

The number of dies produced can be interpreted differently by some suppliers – clarity is needed to define whether the number of dies refers to the number of functional dies produced or the total number of dies. This distinction could become especially important when R&D activities occur at the manufacturing facility.

Other considerations

- *What are the key questions that should be asked of a facility to determine appropriate allocation?*
    - What activities take place at the facility (fabrication, assembly, test, R&D, etc.)? The answer to this question will indicate whether area-based metrics are appropriate.
    - What wafer size or technology node is relevant for the facility? Technology node and wafer size can be indicative of level of complexity of the product, therefore indicating whether area-based allocation is sufficient versus including mask layer information.
- *List any allocation guidance provided by relevant standards, or other similar documents:*
    - International SEMATECH Manufacturing Initiative. “Semiconductor Key Performance Indicators Guidance.” 2009.

Conclusion: Preferred Facility-Level Allocation Method for IC Manufacturing

Because most of the processes in wafer fabrication scale with area, the area of output wafer is the most appropriate way to allocate total facility burden to an individual product. A modification should be made to account for yield in this allocation. For certain facilities it can make sense to further normalize this impact by number of mask layers to reflect the differences in complexity of processes. However, sometimes it can be difficult to know this information.

Consequently, the total manufacturing carbon footprint equation for an IC is as follows:

$$\mathbf{MCF_{IC}\ (kg\ CO2e)} = [GHG_F\ \mathbf{/}\ (A_{output})] * (A_{IC})$$

where…

MCF_{IC} = the manufacturing carbon footprint of a single IC – cradle to gate (kg CO2e)

GHG_F = the total manufacturing facility greenhouse gas emissions in a year (kg CO2e)

A_{output} = the total good wafer out (in cm^2)

A_{IC} = the total area of a specific IC (in cm^2)

Alternatively:

$$\mathbf{MCF_{IC}\ (kg\ CO2e)} = [GHG_F\ \mathbf{/}\ (A_{output} * ML_{fab})] * (A_{IC} * ML_{IC})$$

where…

MCF_{IC} = the manufacturing carbon footprint of a single IC – cradle to gate (kg CO2e)

GHG_F = the total manufacturing facility greenhouse gas emissions in a year (kg CO2e)

A_{output} = the total good wafer out (in cm^2)

ML_{fab} = number of mask layers for the facility

ML_{IC} = number of mask layers for the specific IC

A_{IC} = the total area of a specific IC (in cm^2)