LENOVO® THINKSERVER®
MEMORY RAS TECHNOLOGIES

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MEMORY RAS FEATURES

While advanced ECC provides memory correction, it does not provide failover capability. ThinkServers provide Memory Mirroring and Memory Lockstep to enable failover/backup capability to maintain server availability goals.

ThinkServer	Memory Mirroring	Memory Lock step
TD230	X	
RD230	X	X
RD240	X	X

MEMORY MIRRORING

Memory Mirroring provides full protection against single-bit and multi-bit errors. With Mirrored Memory mode enabled, memory contents are written to two different places in physical system memory (two different channels) simultaneously. If a memory read from one channel returns incorrect data due to an uncorrectable memory error, the system automatically retrieves the data from the other channel. 100% redundancy is assured, but at cost of reduced capacity and performance. When memory mirroring is enabled, the memory capacity available to the operating system is only ½ of what is populated since only one of the two populated channels provides data. Memory performance will also be reduced when memory mirroring is enabled since effectively, only 1 channel of memory is used (the second is used for redundancy). Both mirroring and lock-step will have reduced performance vs. all other configurations; however, mirroring will have slightly better performance than lock-step.

The following applies when in memory mirroring mode:

- 2 memory channels operating as mirrors of each other. Same content is written to both channels simultaneously
- Both channels must be populated identically
- Only half the populated memory is usable as system memory
- Increased reliability vs. lockstep, but max memory capacity drops (you effectively have only one channel of memory both from a capacity standpoint)

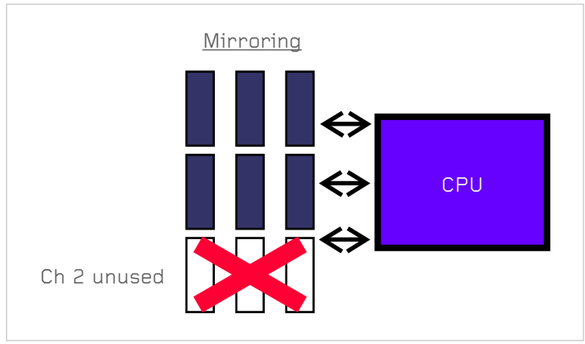

Figure 1 - Typical Memory Mirroring Configuration (one processor)

MEMORY LOCKSTEP

In lockstep mode, two channels operate as a single channel, and are accessed simultaneously, but different contents are written to each. The cache line is split across both channels so different parts of the same cache line are stored in multiple places. This provides 2x 8-bit error detection and 8-bit error correction within a single DRAM. In three-channel memory systems, the third channel is unused and left unpopulated. Memory lockstep reduces the total system memory capacity by a third in 3 DIMM per channel designs.

The following applies when in memory lockstep mode:

- 2 channels operating in lockstep (cache line is split across both channels), 3rd channel is unused
- Both channels must be populated identically
- x8 SDDC is supported (x8 SDDC is supported only in lockstep mode)
- No mirroring support in this mode
- Compared to a 3-channel configuration with only x4 SDDC, reliability increases, but performance drops and capacity drops (only 2 channels used)

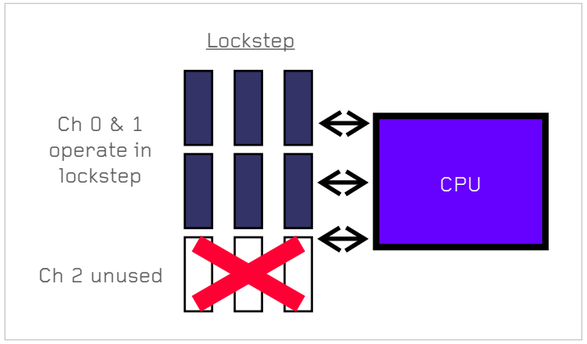

Figure 2 - Typical Memory Lock Step Configuration (one processor)

MEMORY LOCKSTEP VS. MEMORY MIRRORING

So what is the difference, and why choose one of the other? Both mirroring and lockstep provide higher reliability than the other memory configurations (which only provide x4 SDDC). However, with the additional reliability, there are tradeoffs. Both mirroring and lockstep will reduce the performance of the memory subsystem and the amount of memory available in the system by 2/3 for mirroring and by 1/3 for lockstep. Lockstep is lower performance compared to mirroring. The real difference is that lockstep will allow the system to run un-interrupted if a single x8 (or 2 x4) DRAM devices on a DIMM fail, while memory mirroring will continue to operate, uninterrupted, if an entire DIMM fails. Thus Mirroring is a higher reliability solution.

MEMORY POPULATION REQUIREMENTS

Lockstep is lower performance compared to mirroring. The real difference is that lockstep will allow the system to run un-interrupted if a single x8 (or 2 x4) DRAM devices on a DIMM fail, while memory mirroring will continue to operate, uninterrupted, if an entire DIMM fails. Thus Mirroring is a higher reliability solution.

1. Mirrored mode and lockstep mode both require that channel 0 and channel 1 are exact copies of each other
   - › Channels must have DIMMs that are identical in organization (#ranks, #rows, #cols, #banks)
   - › Can run with differently rated DIMMs and use the settings of the slowest DIMM on both channels
   - › Channel 2 is not usable in either of these modes

2. With memory installed behind both sockets of a DP system, both sockets must be running the same RAS mode and paging policy
   - › Only exception is when mirroring redundancy is lost on one socket, this will not force the loss on the other socket

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